Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for partitioning a large computer program ~~programs and or algorithms~~ at least part of which is to be executed by an array of reconfigurable units including a plurality of ~~such as~~ Arithmetic Logic Units (ALUS) and a plurality of memory units, comprising the steps of:

defining a maximum allowable size to be mapped onto the array; and [[,]]

partitioning the program such that its separate parts minimize the overall execution time and provide ~~providing~~ a mapping onto the array not exceeding the maximum allowable size.

2. (Currently Amended) A device for partitioning a large computer program ~~programs and or algorithms~~ at least part of which is to be executed by an array of reconfigurable units including a plurality of ~~such as~~ Arithmetic Logic Units (ALUS) and a plurality of memory units, comprising:

an arrangement [[means]] for defining a maximum allowable size to be mapped onto the array; and [[,]]

an arrangement [[means]] for partitioning the program such that its separate parts minimize the overall execution time and provide ~~for providing~~ a mapping onto the array not exceeding the maximum allowable size.

3. (Currently Amended) A method for partitioning at least one of large computer programs and large algorithms at least part of which is to be executed by an array of reconfigurable ~~processing~~ units, the array including a plurality of memory units, the method comprising:

defining a maximum allowable size to be mapped onto the array;

partitioning at least one of a program and an algorithm such that its separate parts (a) minimize an overall execution time of the at least one of the program and the algorithm and (b) each does not exceed the maximum allowable size; and

mapping the separate parts onto the array.

4. (Currently Amended) The method of claim 3, wherein the array further includes a plurality of reconfigurable ~~processing units are~~ arithmetic logic units.